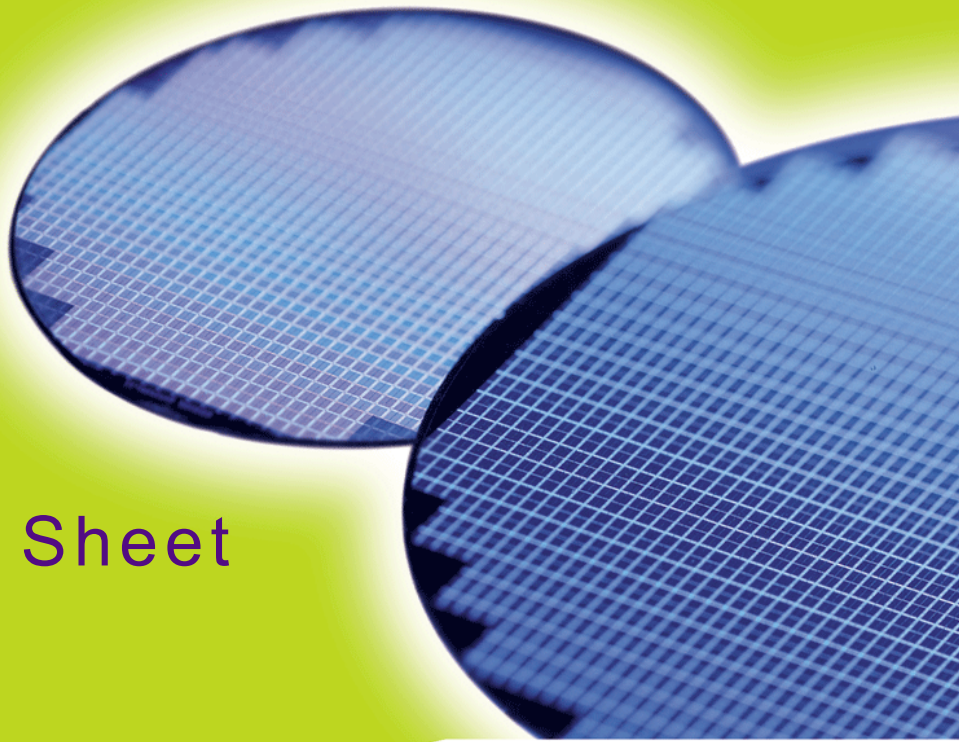


HYB18T512161BF

*512-Mbit x16 DDR2 SDRAM
DDR2 SDRAM
RoHS compliant*



Internet Data Sheet

Rev. 1.43



HYB18T512161BF	
Revision History: 2006-11, Rev. 1.43	
Page	Subjects (major changes since last revision)
All	Adapted internet edition
94-101	added chapter 7 explaining AC timing measurement condition (reference load ; slew rate ; set up & hold timing references ; derating values for input /command ,data)
82-86	setup & hold timings are changed with reference to Industrial standard definition
All	removed all the occurrences of RDQS as it is not used in graphics (x16)
Previous Revision: 2006-09, Rev. 1.32	
All	Qimonda Update
Previous Revision: 2006-03, Rev. 1.31	
9	added power supply info for [-20 and -22]
86	table 41: change I_{DD} max to I_{DD} typ
77 - 80	Corrected AC Timing values for -20 speedsort in table 35 and table 36
Previous Revision: 2006-02, Rev. 1.21	
67	table 18: added speed sort -20
71	table 24: added speed sort -20
76	table 33 and table 34: added speed sort -20
77	table 35: change CL=7 2.0 tCK (speed sort -20)
78	table 36: added all values for speed sort -20
86	table 41: added all IDD values (all speed sorts)

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HYB18T512161BF–20/22/25/28/33
512-Mbit Double-Data-Rate-Two SDRAM

1 Overview

This chapter gives an overview of the 512-Mbit Double-Data-Rate-Two SDRAM product family for graphics application and describes its main characteristics.

1.1 Features

The 512-Mbit Double-Data-Rate-Two SDRAM offers the following key features:

- $1.8\text{ V} \pm 0.1\text{V } V_{DD}$ for [–25/–28/–33]
- $2.0\text{ V} \pm 0.1\text{V } V_{DD}$ for [–20/–22]
- $1.8\text{ V} \pm 0.1\text{V } V_{DDQ}$ for [–25/–28/–33]
- $2.0\text{ V} \pm 0.1\text{V } V_{DDQ}$ for [–20/–22]
- DRAM organizations with 16 data in/outputs
- Double Data Rate architecture:
 - two data transfers per clock cycle
 - four internal banks for concurrent operation
- Programmable CAS Latency: 3, 4, 5, 6, 7
- Programmable Burst Length: 4 and 8
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- Bi-directional, differential data strobes (DQS and $\overline{\text{DQS}}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and DQS transitions with clock
- DQS can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted $\overline{\text{CAS}}$ by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality.
- Auto-Precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Average Refresh Period $7.8\ \mu\text{s}$ at a T_{CASE} lower than $85\ ^\circ\text{C}$, $3.9\ \mu\text{s}$ between $85\ ^\circ\text{C}$ and $95\ ^\circ\text{C}$
- Full Strength and reduced Strength (60%) Data-Output Drivers
- 2kB page size
- Packages: P-TFBGA-84 for $\times 16$ components
- RoHS Compliant Products¹⁾

TABLE 1**Ordering Information for RoHS compliant products**

Product Number	Org.	Clock (MHz)	Package
HYB18T512161BF–20/22/25/28/33	$\times 16$	500/450/400/350/300	P-TFBGA-84

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

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512-Mbit Double-Data-Rate-Two SDRAM

1.2 Description

The 512-Mb DDR2 DRAM is a high-speed Double-Data-Rate-Two CMOS DRAM device containing 536,870,912 bits and internally configured as a quad-bank DRAM. The 512-Mb device is organized as 8 Mbit \times 16 I/O \times 4 banks chip. These devices achieve high speed transfer rates starting at 400 Mb/sec/pin for general applications.

The device is designed to comply with all DDR2 DRAM key features:

1. posted $\overline{\text{CAS}}$ with additive latency,
2. write latency = read latency - 1,
3. normal and weak strength data-output driver,
4. Off-Chip Driver (OCD) impedance adjustment
5. On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are

latched at the cross point of differential clocks (CK rising and $\overline{\text{CK}}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS- $\overline{\text{DQS}}$ pair in a source synchronous fashion.

A 15-bit address bus for $\times 16$ components is used to convey row, column and bank address information in a $\overline{\text{RAS-CAS}}$ multiplexing style.

An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The DDR2 SDRAM is available in P-TFBGA package.



2 Pin Configuration

2.1 Pin Configuration

The pin configuration of a DDR2 SDRAM is listed by function in **Table 2**. The abbreviations used in the Pin#/Buffer Type columns are explained in **Table 3** and **Table 4** respectively. The pin numbering for the FBGA package is depicted in Figure 1 for ×16.

TABLE 2
Pin Configuration of DDR SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals ×16 organization				
J8	CK	I	SSTL	Clock Signal CK, Complementary Clock Signal CK
K8	$\overline{\text{CK}}$	I	SSTL	
K2	CKE	I	SSTL	Clock Enable
Control Signals ×16 organization				
K7	$\overline{\text{RAS}}$	I	SSTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)
L7	$\overline{\text{CAS}}$	I	SSTL	
K3	$\overline{\text{WE}}$	I	SSTL	
L8	$\overline{\text{CS}}$	I	SSTL	Chip Select
Address Signals ×16 organization				
L2	BA0	I	SSTL	Bank Address Bus 1:0
L3	BA1	I	SSTL	
L1	NC	–	–	



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512-Mbit Double-Data-Rate-Two SDRAM

Ball#/Pin#	Name	Pin Type	Buffer Type	Function
M8	A0	I	SSTL	Address Signal 12:0,Address Signal 10/Autoprecharge
M3	A1	I	SSTL	
M7	A2	I	SSTL	
N2	A3	I	SSTL	
N8	A4	I	SSTL	
N3	A5	I	SSTL	
N7	A6	I	SSTL	
P2	A7	I	SSTL	
P8	A8	I	SSTL	
P3	A9	I	SSTL	
M2	A10	I	SSTL	
	AP	I	SSTL	
P7	A11	I	SSTL	
R2	A12	I	SSTL	
Data Signals ×16 organization				
G8	DQ0	I/O	SSTL	Data Signal 15:0 <i>Note: Bi-directional data bus. DQ[15:0] for ×16 components</i>
G2	DQ1	I/O	SSTL	
H7	DQ2	I/O	SSTL	
H3	DQ3	I/O	SSTL	
H1	DQ4	I/O	SSTL	
H9	DQ5	I/O	SSTL	
F1	DQ6	I/O	SSTL	
F9	DQ7	I/O	SSTL	
C8	DQ8	I/O	SSTL	
C2	DQ9	I/O	SSTL	
D7	DQ10	I/O	SSTL	
D3	DQ11	I/O	SSTL	
D1	DQ12	I/O	SSTL	
D9	DQ13	I/O	SSTL	
B1	DQ14	I/O	SSTL	
B9	DQ15	I/O	SSTL	
Data Strobe ×16 organization				
B7	UDQS	I/O	SSTL	Data Strobe Upper Byte
A8	$\overline{\text{UDQS}}$	I/O	SSTL	
F7	LDQS	I/O	SSTL	Data Strobe Lower Byte
E8	$\overline{\text{LDQS}}$	I/O	SSTL	



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Ball#/Pin#	Name	Pin Type	Buffer Type	Function
Data Mask ×16 organization				
B3	UDM	I	SSTL	Data Mask Upper Byte
F3	LDM	I	SSTL	Data Mask Lower Byte
Power Supplies ×16 organizations				
A9,C1,C3,C7,C9	V_{DDQ}	PWR	–	I/O Driver Power Supply
A1	V_{DD}	PWR	–	Power Supply
A7,B2,B8,D2,D8	V_{SSQ}	PWR	–	Power Supply
A3,E3	V_{SS}	PWR	–	Power Supply
Power Supplies ×16 organization				
J2	V_{REF}	AI	–	I/O Reference Voltage
E9, G1, G3, G7, G9	V_{DDQ}	PWR	–	I/O Driver Power Supply
J1	V_{DDL}	PWR	–	Power Supply
E1, J9, M9, R1	V_{DD}	PWR	–	Power Supply
E7, F2, F8, H2, H8	V_{SSQ}	PWR	–	Power Supply
J7	V_{SSDL}	PWR	–	Power Supply
J3,N1,P9	V_{SS}	PWR	–	Power Supply
Not Connected ×16 organization				
A2, E2, L1, R3, R7, R8	NC	NC	–	Not Connected
Other Pins ×16 organization				
K9	ODT	I	SSTL	On-Die Termination Control

TABLE 3
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

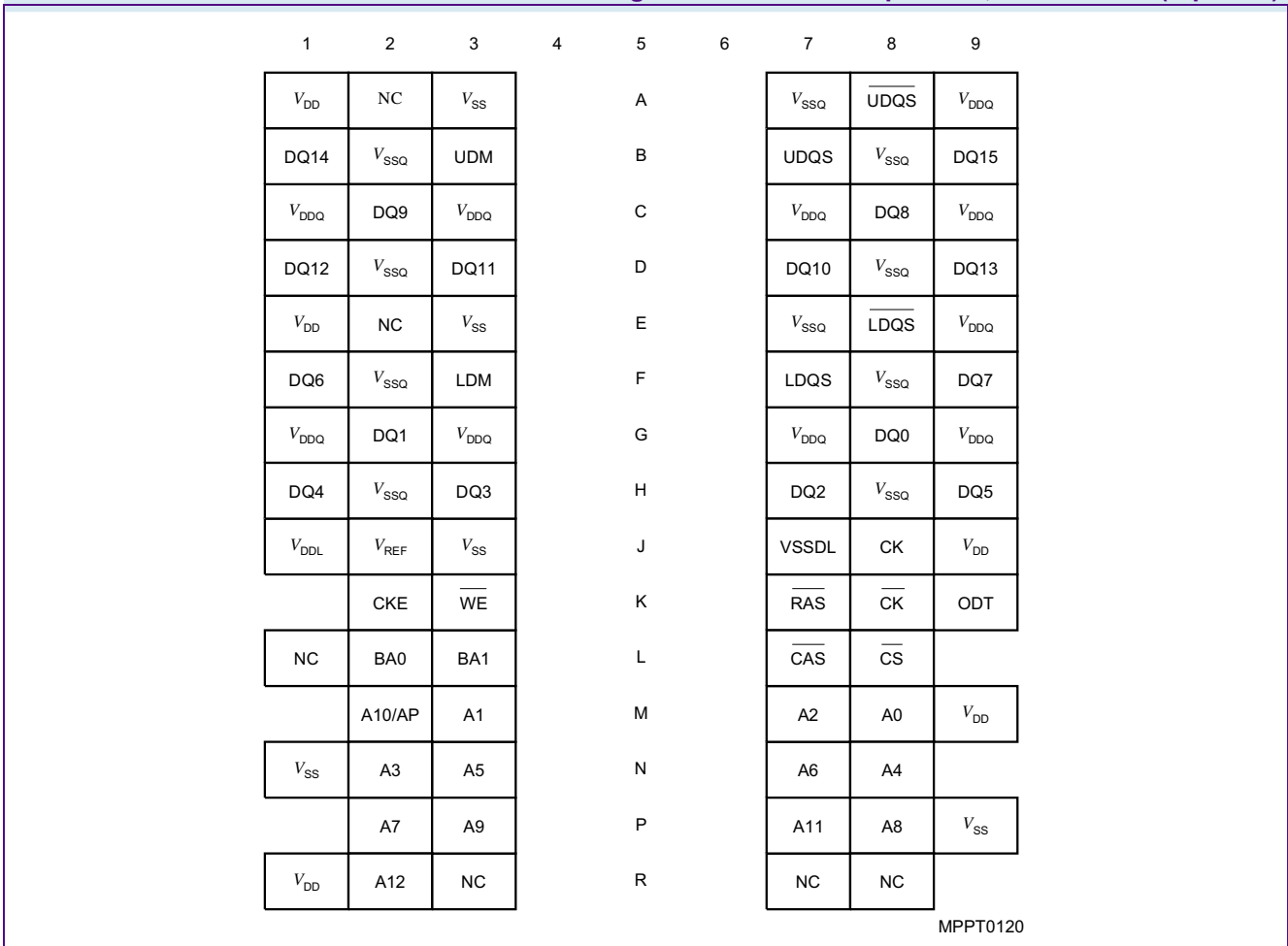


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TABLE 4
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1
Pin Configuration for ×16 components, P-TFBGA-84 (top view)



Note:

- UDQS/ \overline{UDQS} is data strobe for DQ[15:8], LDQS/ \overline{LDQS} is data strobe for DQ[7:0]
- LDM is the data mask signal for DQ[7:0], UDM is the data mask signal for DQ[15:8]
- V_{DDL} and V_{DDSL} are power and ground for the DLL. They are isolated on the device from V_{DD} , V_{DDQ} , V_{SS} and V_{SSQ} .

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2.2 512 Mbit DDR2 Addressing

TABLE 5
512-Mbit DDR2 Addressing

Configuration	32-Mbit x 16	Note
Bank Address	BA[1:0]	
Number of Banks	4	
Auto-Precharge	A10 / AP	
Row Address	A[12:0]	
Column Address	A[9:0]	
Number of Column Address Bits	10	1)
Number of I/Os	16	2)
Page Size [Bytes]	2048 (2K)	3)

1) Referred to as 'colbits'

2) Referred to as 'org'

3) $PageSize = 2^{colbits} \times org / 8$ [Bytes]



3 Functional Description

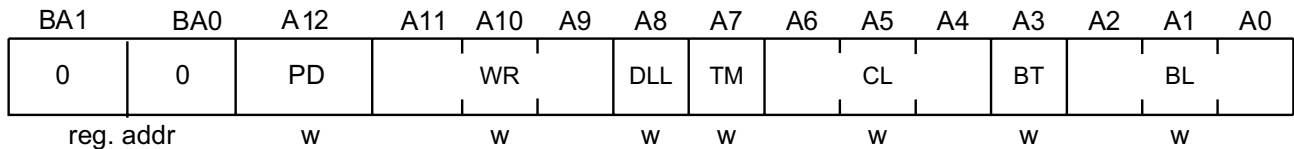


TABLE 6
Mode Register Definition (BA[1:0] = 00B)

Field	Bits	Type ¹⁾	Description
BA1	14	reg. addr.	Bank Address [1] 0 _B BA1 Bank Address
BA0	13		Bank Address [0] 0 _B BA0 Bank Address
PD	12	w	Active Power-Down Mode Select 0 _B PD Fast exit 1 _B PD Slow exit
WR	[11:9]	w	Write Recovery²⁾ <i>Note: All other bit combinations are illegal.</i> 001 _B WR 2 010 _B WR 3 011 _B WR 4 100 _B WR 5 101 _B WR 6
DLL	8	w	DLL Reset 0 _B DLL No 1 _B DLL Yes
TM	7	w	Test Mode 0 _B TM Normal Mode 1 _B TM Vendor specific test mode
CL	[6:4]	w	CAS Latency <i>Note: All other bit combinations are illegal.</i> 010 _B CL reserved 011 _B CL 3 100 _B CL 4 101 _B CL 5 110 _B CL 6 111 _B CL 7

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Field	Bits	Type ¹⁾	Description
BT	3	w	Burst Type 0 _B BT Sequential 1 _B BT Interleaved
BL	[2:0]	w	Burst Length <i>Note: All other bit combinations are illegal.</i> 010 _B BL 4 011 _B BL 8

1) w = write only register bits

2) Number of clock cycles for write recovery during auto-precharge. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: $WR [cycles] \geq t_{WR} (ns) / t_{CK} (ns)$. The mode register must be programmed to fulfill the minimum requirement for the analogue t_{WR} timing WR_{MIN} is determined by $t_{CK,MAX}$ and WR_{MAX} is determined by $t_{CK,MIN}$.



BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Q _{off}	0	$\overline{\text{DQS}}$	OCD Program			R _{tt}	AL			R _{tt}	DIC	DLL
reg. addr				w		w		w		w		w	w	w

TABLE 7

Extended Mode Register Definition (BA[1:0] = 01B)

Field	Bits	Type ¹⁾	Description
BA1	14	reg. addr.	Bank Address [1] 0 _B BA1 Bank Address
BA0	13		Bank Address [0] 0 _B BA0 Bank Address
Qoff	12	w	Output Disable 0 _B QOff Output buffers enabled 1 _B QOff Output buffers disabled
$\overline{\text{DQS}}$	10		Complement Data Strobe (DQS Output) 0 _B DQS Enable 1 _B DQS Disable
OCD Program	[9:7]		Off-Chip Driver Calibration Program 000 _B OCD OCD calibration mode exit, maintain setting 001 _B OCD Drive (1) 010 _B OCD Drive (0) 100 _B OCD Adjust mode 111 _B OCD OCD calibration default
AL	[5:3]		Additive Latency <i>Note: All other bit combinations are illegal.</i> 000 _B AL 0 001 _B AL 1 010 _B AL 2 011 _B AL 3 100 _B AL 4 101 _B AL 5 110 _B AL 6
R _{TT}	2,6		Nominal Termination Resistance of ODT 00 _B RTT ∞ (ODT disabled) 01 _B RTT 75 Ohm 10 _B RTT 150 Ohm 11 _B RTT 50 Ohm
DIC	1		Off-chip Driver Impedance Control 0 _B DIC Full (Driver Size = 100%) 1 _B DIC Reduced
DLL	0		DLL Enable 0 _B DLL Enable 1 _B DLL Disable

1) w = write only register bits



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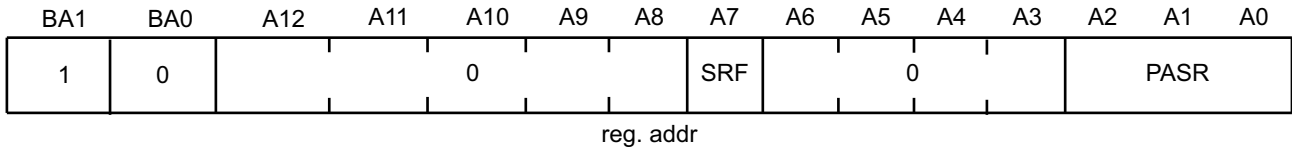


TABLE 8

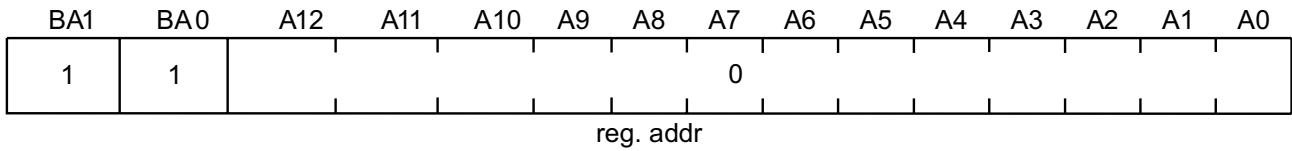
EMRS(2) Programming Extended Mode register Definition (BA[1:0]=10_B)

Field	Bits	Type ¹⁾	Description
BA	[14:13]	w	Bank Address[14:13] 00 _B BA MRS 01 _B BA EMRS(1) 10 _B BA EMRS(2) 11 _B BA EMRS(3): Reserved
A	[12:8]	w	Address Bus[12:8] 0 _B A[12:8] Address bits
A	7	w	Address Bus[7] <i>Note: adapted self refresh rate for Tcase > 85 °C</i> 0 _B A7 disable 1 _B A7 enable ²⁾³⁾
A	[6:3]	w	Address Bus[6:3] 0 _B A[6:3] Address bits
Partial Self Refresh for 4 banks			
A	[2:0]	w	Address Bus[2:0], Partial Array Self Refresh for 4 Banks 000 _B PASR0 Full Array 001 _B PASR1 Half Array (BA[1:0]=00, 01) 010 _B PASR2 Quarter Array (BA[1:0]=00) 011 _B PASR3 Not defined 100 _B PASR4 3/4 array (BA[1:0]=01, 10, 11) 101 _B PASR5 Half array (BA[1:0]=10, 11) 110 _B PASR6 Quarter array (BA[1:0]=11) 111 _B PASR7 Not defined

- 1) w = write only
- 2) When DRAM is operated at $85C \leq T_{Case} \leq 95C$ the extended self refresh rate must be enabled by setting bit A7 to "1" before the self refresh mode can be entered.
- 3) If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified location will be lost if self refresh is entered. Data integrity will be maintained if tREF conditions are met and no Self Refresh command is issued



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MPBT0400

TABLE 9

EMR(3) Programming Extended Mode Register Definition (BA[1:0]=10_B)

Field	Bits	Type ¹⁾	Description
BA1	14		Bank Address[1] 1 _B BA1 Bank Address
BA0	13		Bank Address[0] 1 _B BA0 Bank Address
A	[12:0]	w	Address Bus[12:0] 0 _B A[12:0] Address bits

1) w = write only

TABLE 10

ODT Truth Table

Input Pin	EMRS(1) Address Bit A10	EMRS(1) Address Bit A11
x16 components		
DQ[7:0]	X	
DQ[15:8]	X	
LDQS	X	
$\overline{\text{LDQS}}$	0	X
UDQS	X	
$\overline{\text{UDQS}}$	0	X
LDM	X	
UDM	X	

Note: X = don't care; 0 = bit set to low; 1 = bit set to high



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512-Mbit Double-Data-Rate-Two SDRAM

TABLE 11
Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x 0 0	0, 1, 2, 3	0, 1, 2, 3
	x 0 1	1, 2, 3, 0	1, 0, 3, 2
	x 1 0	2, 3, 0, 1	2, 3, 0, 1
	x 1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Notes

1. *PageSize and Length is a function of I/O organization: 32Mb x 16 organization (CA[9:0]); Page Size = 2 kByte; Page Length = 1024*

2. *Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components*



4 Truth Tables

TABLE 12
Command Truth Table

Function	CKE		\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0 BA1	A[13:11]	A10	A[9:0]	Note ¹⁾²⁾³⁾
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			4)5)
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	4)
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	4)6)
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	4)6)7)
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	4)5)
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	4)
Bank Activate	H	H	L	L	H	H	BA	Row Address			4)5)
Write	H	H	L	H	L	L	BA	Column	L	Column	4)5)8)
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	4)5)8)
Read	H	H	L	H	L	H	BA	Column	L	Column	4)5)8)
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	4)5)8)
No Operation	H	X	L	H	H	H	X	X	X	X	4)
Device Deselect	H	X	H	X	X	X	X	X	X	X	4)
Power Down Entry	H	L	H	X	X	X	X	X	X	X	4)9)
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	4)9)
			L	H	H	H					

- 1) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- 2) "X" means "H or L (but a defined logic level)".
- 3) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) All DDR2 SDRAM commands are defined by states of \overline{CS} , \overline{WE} , \overline{RAS} , \overline{CAS} , and CKE at the rising edge of the clock.
- 5) Bank addresses BA[1:0] determine which bank is to be operated upon. For (E)MRS BA[1:0] selects an (Extended) Mode Register.
- 6) V_{REF} must be maintained during Self Refresh operation.
- 7) Self Refresh Exit is asynchronous.
- 8) Burst reads or writes at BL = 4 cannot be terminated.
- 9) The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements.



TABLE 13

Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State ¹⁾	CKE		Command (N) ²⁾³⁾ RAS, CAS, WE, CS	Action (N) ²⁾	Note ⁴⁾⁵⁾
	Previous Cycle ⁶⁾ (N-1)	Current Cycle ⁶⁾ (N)			
Power-Down	L	L	X	Maintain Power-Down	7)8)11)
	L	H	DESELECT or NOP	Power-Down Exit	7)9)10)11)
Self Refresh	L	L	X	Maintain Self Refresh	8)11)12)
	L	H	DESELECT or NOP	Self Refresh Exit	9)12)13)14)
Bank(s)Active	H	L	DESELECT or NOP	Active Power-Down Entry	7)9)10)11)15)
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	9)10)11)15)
	H	L	AUTOREFRESH	Self Refresh Entry	7)11)14)16)
Any State other than listed above	H	H	Refer to the Command Truth Table		17)

- 1) Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
- 2) Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N)
- 3) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- 4) CKE must be maintained HIGH while the device is in OCD calibration mode.
- 5) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 6) CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- 7) The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements
- 8) "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).
- 9) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- 10) Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
- 11) t_{CKE_MIN} of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2 \times t_{CKE} + t_{IH}$.
- 12) V_{REF} must be maintained during Self Refresh operation.
- 13) On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
- 14) Valid commands for Self Refresh Exit are NOP and DESELCT only.
- 15) Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress.
- 16) Self Refresh mode can only be entered from the All Banks Idle state.
- 17) Must be a legal command as defined in the Command Truth Table.

TABLE 14

Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

- 1) Used to mask write data; provided coincident with the corresponding data.



5 Electrical Characteristics

TABLE 15

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Unit	Note
T_{CASE}	Operating Temperature	0 to 95	°C	1)2)3)4)

- 1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
- 2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
- 3) Above 85 °C case temperature the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$.
- 4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. Note, when the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

5.1 Absolute Maximum Ratings

TABLE 16

Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		min.	max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0	2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5	2.3	V	1)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	-0.5	2.3	V	1)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5	2.3	V	1)
T_J	Junction Temperature	—	125	°C	1)
T_{STG}	Storage Temperature	-55	150	°C	1)2)

- 1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.



5.2 DC Characteristics

TABLE 17
Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1)2)
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1)2)
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1)2)
V_{DD}	Supply Voltage	1.9	2.0	2.1	V	2)3)
V_{DDDL}	Supply Voltage for DLL	1.9	2.0	2.1	V	2)3)
V_{DDQ}	Supply Voltage for Output	1.9	2.0	2.1	V	2)3)
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	4)5)
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	6)

- 1) HYB18T512161BF–[25/28/33]
- 2) V_{DDQ} tracks with V_{DD} , V_{DDDL} tracks with V_{DD} . AC parameters are measured with V_{DD} , V_{DDQ} and V_{DDDL} tied together.
- 3) HYB18T512161BF–[20/22]
- 4) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ} .
- 5) Peak to peak ac noise on V_{REF} may not exceed $\pm 2\% V_{REF}$ (dc)
- 6) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in die dc level of V_{REF} .

TABLE 18
ODT DC Electrical Characteristics

Parameter / Condition	Symbol	Min.	Nom.	Max.	Unit	Note
Termination resistor impedance value for EMRS(1)[A6,A2] = [0,1]; 75 Ohm	Rtt1(eff)	60	75	90	Ω	1)
Termination resistor impedance value for EMRS(1)[A6,A2] = [1,0]; 150 Ohm	Rtt2(eff)	120	150	180	Ω	1)
Termination resistor impedance value for EMRS(1)(A6,A2)=[1,1]; 50 Ohm	Rtt3(eff)	40	50	60	Ω	1)
Deviation of V_M with respect to $V_{DDQ} / 2$	delta V_M	-6.00	—	+ 6.00	%	2)

- 1) Measurement Definition for Rtt(eff): Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IH(ac)})$ and $I(V_{IL(ac)})$ respectively.
 $Rtt(eff) = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IH(ac)}) - I(V_{IL(ac)}))$.
- 2) Measurement Definition for V_M : Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load: $delta V_M = ((2 \times V_M / V_{DDQ}) - 1) \times 100\%$



TABLE 19
Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Unit	Note
IIL	Input Leakage Current; any input $0\text{ V} < V_{IN} < V_{DD}$	-2	+2	μA	1)
IOL	Output Leakage Current; $0\text{ V} < V_{OUT} < V_{DDQ}$	-5	+5	μA	2)

- 1) all other pins not under test = 0 V
- 2) DQ's, LDQS, LDQS, UDQS, UDQS, DQS, $\overline{\text{DQS}}$ are disabled and ODT is turned off

5.3 DC & AC Characteristics

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF} .

In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{\text{DQS}}$. This distinction in timing methods is verified by design and characterization but not subject to production test. In single ended mode, the $\overline{\text{DQS}}$ signals are internally disabled and don't care.

TABLE 20
DC & AC Logic Input Levels

Symbol	Parameter	Min.	Max.	Units
$V_{IH(dc)}$	DC input logic high	$V_{REF} + 0.125$	$V_{DDQ} + 0.3$	V
$V_{IL(dc)}$	DC input low	-0.3	$V_{REF} - 0.125$	V
$V_{IH(ac)}$	AC input logic high	$V_{REF} + 0.250$	—	V
$V_{IL(ac)}$	AC input low	—	$V_{REF} - 0.250$	V

TABLE 21
Single-ended AC Input Test Conditions

Symbol	Condition	Value	Unit	Note
V_{REF}	Input reference voltage	$0.5 \times V_{DDQ}$	V	1)
$V_{SWING.MAX}$	Input signal maximum peak to peak swing	1.0	V	1)
SLEW	Input signal minimum Slew Rate	1.0	V / ns	2)3)

- 1) Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
- 2) The input signal minimum Slew Rate is to be maintained over the range from $V_{IH(ac).MIN}$ to V_{REF} for rising edges and the range from V_{REF} to $V_{IL(ac).MAX}$ for falling edges as shown in **Figure 2**
- 3) AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.



FIGURE 2
Single-ended AC Input Test Conditions Diagram

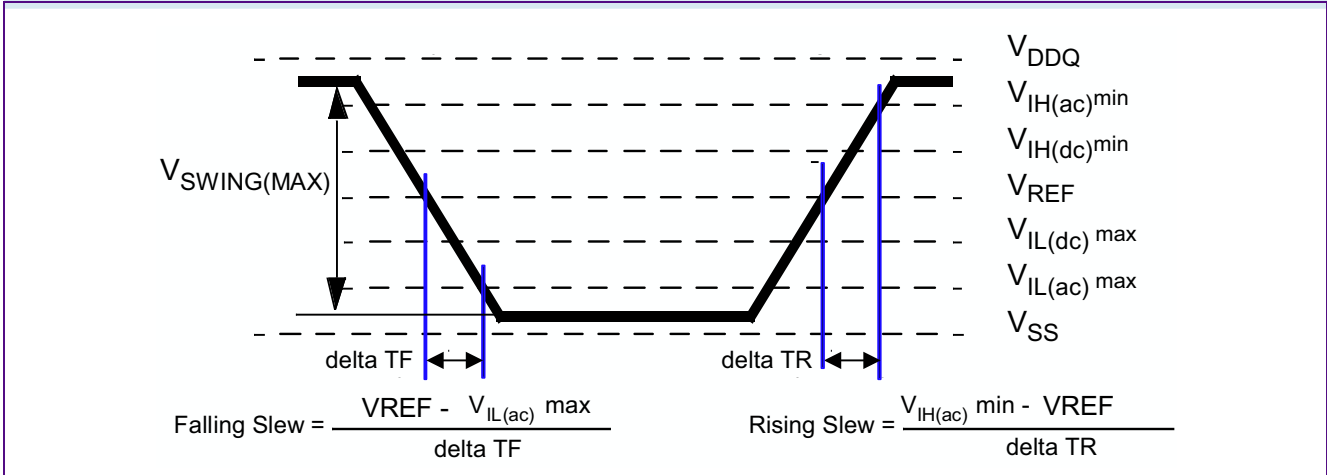
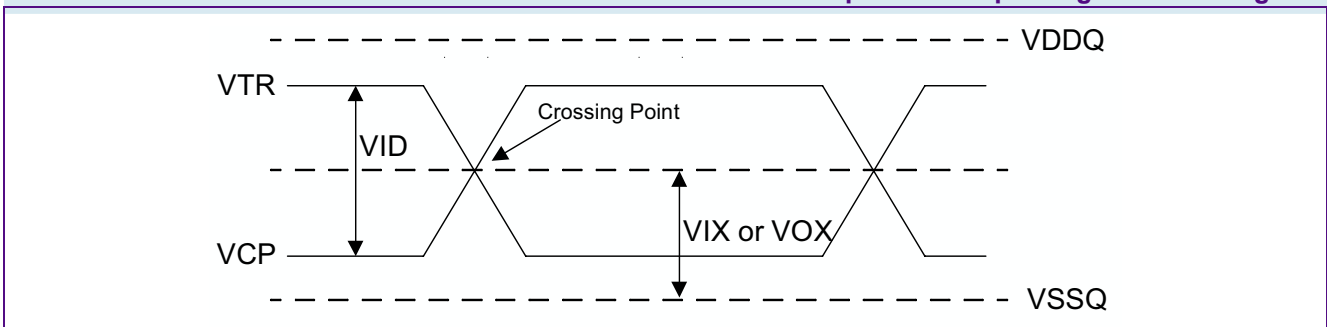


TABLE 22
Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	Min.	Max.	Unit	Note
$V_{IN(dc)}$	DC input signal voltage	-0.3	$V_{DDQ} + 0.3$	—	1)
$V_{ID(dc)}$	DC differential input voltage	0.25	$V_{DDQ} + 0.6$	—	2)
$V_{ID(ac)}$	AC differential input voltage	0.5	$V_{DDQ} + 0.6$	V	3)
$V_{IX(ac)}$	AC differential cross point input voltage	$0.5 \times V_{DDQ} - 0.175$	$0.5 \times V_{DDQ} + 0.175$	V	4)
$V_{OX(ac)}$	AC differential cross point output voltage	$0.5 \times V_{DDQ} - 0.125$	$0.5 \times V_{DDQ} + 0.125$	V	5)

- 1) $V_{IN(dc)}$ specifies the allowable DC execution of each input of differential pair such as CK, \overline{CK} , DQS, \overline{DQS} etc.
- 2) $V_{ID(dc)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(dc)} - V_{IL(dc)}$.
- 3) $V_{ID(ac)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(ac)} - V_{IL(ac)}$.
- 4) The value of $V_{IX(ac)}$ is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ} . $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross.
- 5) The value of $V_{OX(ac)}$ is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ} . $V_{OX(ac)}$ indicates the voltage at which differential input signals must cross.

FIGURE 3
Differential DC and AC Input and Output Logic Levels Diagram





5.4 Output Buffer Characteristics

TABLE 23**Full Strength Calibrated Pull-up Driver Characteristics**

Voltage (V)	Calibrated Pull-up Driver Current [mA]				
	Nominal Minimum ¹⁾ (21 Ohms)	Nominal Low ²⁾ (18.75 Ohms)	Nominal ³⁾ (18 ohms)	Nominal High ²⁾ (17.25 Ohms)	Nominal Maximum ⁴⁾ (15 Ohms)
0.2	-9.5	-10.7	-11.4	-11.8	-13.3
0.3	-14.3	-16.0	-16.5	-17.4	-20.0
0.4	-18.3	-21.0	-21.2	-23.0	-27.0

- 1) The driver characteristics evaluation conditions are Nominal Minimum 95 °C (T_{CASE}), $V_{DDQ} = 1.7$ V, any process
- 2) The driver characteristics evaluation conditions are Nominal Low and Nominal High 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, any process
- 3) The driver characteristics evaluation conditions are Nominal 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, typical process
- 4) The driver characteristics evaluation conditions are Nominal Maximum 0 °C (T_{CASE}), $V_{DDQ} = 1.9$ V, any process

TABLE 24**Full Strength Calibrated Pull-down Driver Characteristics**

Voltage (V)	Calibrated Pull-down Driver Current [mA]				
	Nominal Minimum ¹⁾ (21 Ohms)	Nominal Low ²⁾ (18.75 Ohms)	Nominal ³⁾ (18 ohms)	Nominal High ²⁾ (17.25 Ohms)	Nominal Maximum ⁴⁾ (15 Ohms)
0.2	9.5	10.7	11.5	11.8	13.3
0.3	14.3	16.0	16.6	17.4	20.0
0.4	18.7	21.0	21.6	23.0	27.0

- 1) The driver characteristics evaluation conditions are Nominal Minimum 95 °C (T_{CASE}), $V_{DDQ} = 1.7$ V, any process
- 2) The driver characteristics evaluation conditions are Nominal Low and Nominal High 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, any process
- 3) The driver characteristics evaluation conditions are Nominal 25 °C (T_{CASE}), $V_{DDQ} = 1.8$ V, typical process
- 4) The driver characteristics evaluation conditions are Nominal Maximum 0 °C (T_{CASE}), $V_{DDQ} = 1.9$ V, any process



5.5 Input / Output Capacitance

TABLE 25
Input / Output Capacitance

Symbol	Parameter	Min.	Max.	Unit
CCK	Input capacitance, CK and $\overline{\text{CK}}$	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{\text{CK}}$	—	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	1.75	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{\text{DQS}}$	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{\text{DQS}}$	—	0.5	pF



5.6 Overshoot and Undershoot Specification

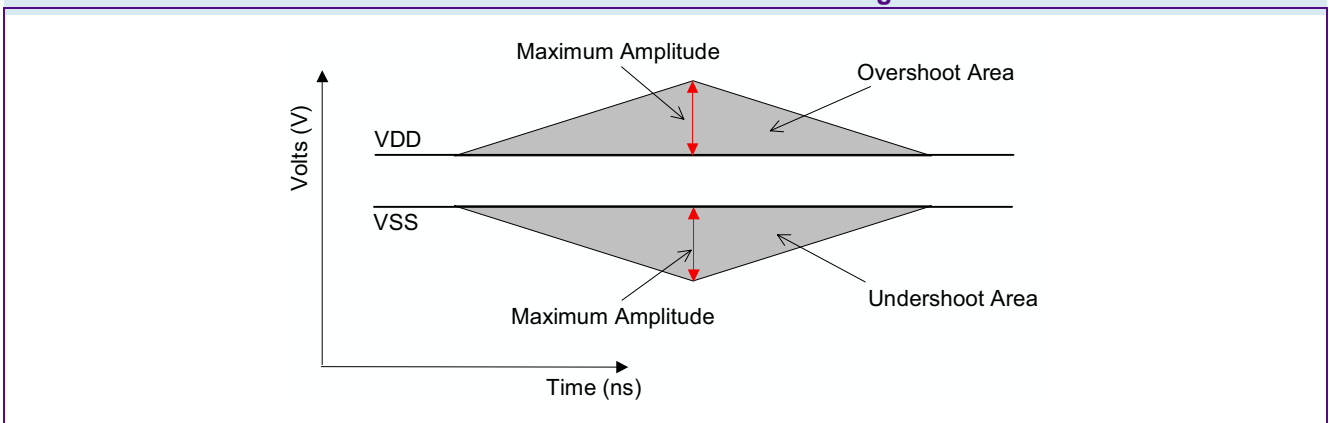
TABLE 26

AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	-20	-22	-25	-28	-33	Unit
Maximum peak amplitude allowed for overshoot area	0.5	0.5	0.5	0.5	0.5	V
Maximum peak amplitude allowed for undershoot area	0.5	0.5	0.5	0.5	0.5	V
Maximum overshoot area above V_{DD}	0.80	0.80	0.80	0.80	0.80	V.ns
Maximum undershoot area below V_{SS}	0.80	0.80	0.80	0.80	0.80	V.ns

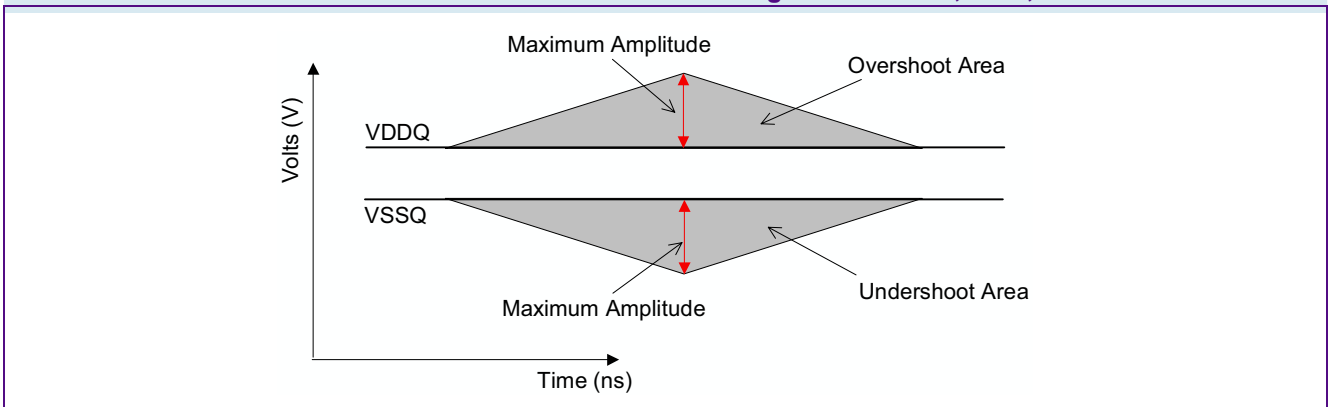
FIGURE 4

AC Overshoot / Undershoot Diagram for Address and Control Pins



HYB18T512161BF-20/22/25/28/33
512-Mbit Double-Data-Rate-Two SDRAM**TABLE 27**
AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	-20	-22	-25	-28	-33	Unit
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	0.9	0.9	V
Maximum overshoot area above V_{DDQ}	0.23	0.23	0.23	0.23	0.23	V.ns
Maximum undershoot area below V_{SSQ}	0.23	0.23	0.23	0.23	0.23	V.ns

FIGURE 5
AC Overshoot / Undershoot Diagram for Clock, Data, Strobe and Mask Pins



5.7 AC Characteristics

5.7.1 Speed Grade Definitions

TABLE 28
Speed Grade Definition

Speed Grade			-20		-22		-25		-28		-33		Unit	Note
Parameter		Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Clock Frequency	@ CL = 3	t_{CK}	3.75	8	3.75	8	3.75	8	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	3.75	8	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3	8	3	8	3	8	3.33	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	2.5	8	2.5	8	2.8	8	3.33	8	ns	1)2)3)4)
	@ CL = 7	t_{CK}	2.0	8	2.2	8	—	—	—	—	—	—	ns	1)2)3)4)
Row Active Time	t_{RAS}	45	70k	45	70k	45	70k	45	70k	45	70k	ns	1)2)3)4) 5)	
Row Cycle Time	t_{RC}	60	—	60	—	60	—	60	—	60	—	ns	1)2)3)4)	
RAS-CAS-Delay	t_{RCD}	15	—	15	—	15	—	15	—	15	—	ns	1)2)3)4)	
Row Precharge Time	t_{RP}	15	—	15	—	15	—	15	—	15	—	ns	1)2)3)4)	

- 1) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 7**. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0).
- 2) The CK/ \overline{CK} input reference level (for timing reference to CK/ \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.



5.7.2 AC Timing Parameters

List of Timing Parameters

TABLE 29

Timing Parameter by Speed Grade

Parameter	Symbol	–20		–22		–25		Unit	Note ¹⁾ 2)3)4)5)6)
		Min.	Max.	Min.	Max.	Min.	Max.		
DQ output access time from CK / CK	t_{AC}	–450	+450	–450	+450	–500	+500	ps	
CAS A to CAS B command period	t_{CCD}	2	—	2	—	2	—	t_{CK}	
CK, \overline{CK} high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	3	—	t_{CK}	
CK, \overline{CK} low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	⁷⁾¹⁸⁾
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	$t_{IS} + t_{CK} + t_{IH}$	—	$t_{IS} + t_{CK} + t_{IH}$	—	ns	⁸⁾
DQ and DM input hold time (differential data strobe)	t_{DH}	145	—	220	—	250	—	ps	⁹⁾
DQ and DM input hold time (single ended data strobe)	t_{DH1}	–105	—	–30	—	0	—	ps	⁹⁾
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	0.35	—	t_{CK}	
DQS output access time from CK / CK	t_{DQSCK}	–450	+450	–450	+450	–500	+500	ps	⁹⁾
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	450	—	450	—	450	ps	¹⁰⁾
Write command to 1st DQS latching transition	t_{DQSS}	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}	20	—	95	—	125	—	ps	⁹⁾
DQ and DM input setup time (single ended data strobe)	t_{DS1}	–105	—	–30	—	0	—	ps	⁹⁾
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		MIN. (t_{CL}, t_{CH})		MIN. (t_{CL}, t_{CH})		—	¹¹⁾
Data-out high-impedance time from CK / CK	t_{HZ}	—	$t_{AC,MAX}$	—	$t_{AC,MAX}$	—	$t_{AC,MAX}$	ps	¹²⁾



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Parameter	Symbol	–20		–22		–25		Unit	Note ¹⁾ 2)3)4)5)6)
		Min.	Max.	Min.	Max.	Min.	Max.		
Address and control input hold time	t_{IH}	525	—	525	—	575	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}	400	—	400	—	450	—	ps	
DQ low-impedance time from CK / CK	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	12)
DQS low-impedance from CK / CK	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	12)
Mode register set command cycle time	t_{MRD}	2	—	2	—	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	0	12	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	—	
Data hold skew factor	t_{QHS}	—	600	—	600	—	600	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	—	7.8	μs	13)14)
		—	3.9	—	3.9	—	3.9	μs	13)15)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	105	—	105	—	ns	16)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	12)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	12)
Active bank A to Active bank B command period	t_{RRD}	10	—	10	—	10	—	ns	14)17)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	7.5	—	ns	
Write preamble	t_{WPRE}	$0.35 \times t_{CK}$	—	$0.35 \times t_{CK}$	—	$0.35 \times t_{CK}$	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	17)
Write recovery time for write without Auto-Precharge	t_{WR}	13	—	13	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{WR}/t_{CK}	—	t_{WR}/t_{CK}	—	t_{CK}	18)
Internal Write to Read command delay	t_{WTR}	7.5	—	7.5	—	7.5	—	ns	19)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	2	—	t_{CK}	20)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	10 – AL	—	9 – AL	—	8 – AL	—	t_{CK}	20)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	2	—	t_{CK}	



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Parameter	Symbol	–20		–22		–25		Unit	Note ¹⁾ 2)3)4)5)6)
		Min.	Max.	Min.	Max.	Min.	Max.		
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	$t_{RFC} + 10$	—	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	200	—	200	—	t_{CK}	

- 1) V_{DDQ} , V_{DD} refer to **Chapter 1**.
- 2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 3) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 5** of this data sheet.
- 4) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/ \overline{CK} , DQS / \overline{DQS} is defined in **Chapter 5.3** of this data sheet.
- 5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 6) The output timing reference voltage level is V_{TT} . See **Chapter 5** for the reference load for timing measurements.
- 7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required.
- 9) timing is referenced to Industrial standard definition
- 10) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ in any given cycle.
- 11) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
- 12) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 13) The Auto-Refresh command interval has been reduced to 3.9 μ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 14) $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 15) $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 16) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 17) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 18) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 19) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 20) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 = “1”) a slow power-down exit timing t_{XARDS} has to be satisfied.



TABLE 30
Timing Parameter by Speed Grade

Parameter	Symbol	–28		–33		Unit	Note ¹⁾ 2)3)4)5)6)
		Min.	Max.	Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	t_{AC}	–550	+550	–600	+600	ps	
CAS A to $\overline{\text{CAS}}$ B command period	t_{CCD}	2	—	2	—	t_{CK}	
CK, $\overline{\text{CK}}$ high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	t_{CK}	
CK, $\overline{\text{CK}}$ low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	7)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	t_{DH}	275	—	295	—	ps	9)
DQ and DM input hold time (single ended data strobe)	t_{DH1}	25	—	45	—	ps	9)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{\text{CK}}$	t_{DQSCK}	–550	+550	–600	+600	ps	9)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	450	—	450	ps	10)
Write command to 1st DQS latching transition	t_{DQSS}	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}	150	—	170	—	ps	9)
DQ and DM input setup time (single ended data strobe)	t_{DS1}	25	—	45	—	ps	9)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})		MIN. (t_{CL}, t_{CH})		—	11)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	t_{HZ}	—	$t_{AC,MAX}$	—	$t_{AC,MAX}$	ps	12)
Address and control input hold time	t_{IH}	625	—	675	—	ps	
Address and control input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}	500	—	550	—	ps	
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ(DQ)}$	2 × $t_{AC,MIN}$	$t_{AC,MAX}$	2 × $t_{AC,MIN}$	$t_{AC,MAX}$	ps	12)
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ(DQS)}$	$t_{AC,MIN}$	$t_{AC,MAX}$	$t_{AC,MIN}$	$t_{AC,MAX}$	ps	12)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	—	
Data hold skew factor	t_{QHS}	—	600	—	600	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	μs	13)14)
		—	3.9	—	3.9	μs	13)15)



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Parameter	Symbol	–28		–33		Unit	Note ¹⁾ 2)3)4)5)6)
		Min.	Max.	Min.	Max.		
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	105	—	105	—	ns	16)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	12)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	12)
Active bank A to Active bank B command period	t_{RRD}	10	—	10	—	ns	14)17)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	
Write preamble	t_{WPRE}	$0.35 \times t_{CK}$	—	$0.35 \times t_{CK}$	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	17)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	15	—	ns	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}	—	t_{WR}/t_{CK}	—	t_{CK}	18)
Internal Write to Read command delay	t_{WTR}	7.5	—	7.5	—	ns	19)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	t_{CK}	20)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	6 – AL	—	t_{CK}	20)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	$t_{RFC} + 10$	—	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	200	—	t_{CK}	

- 1) V_{DDQ} , V_{DD} refer to **Chapter 1**.
- 2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 3) Timings are guaranteed with CK/\overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 5** of this data sheet.
- 4) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/\overline{CK} , DQS / \overline{DQS} is defined in **Chapter 5.3** of this data sheet.
- 5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 6) The output timing reference voltage level is V_{TT} . See **Chapter 5** for the reference load for timing measurements.
- 7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required.
- 9) timing is referenced to Industrial standard definition
- 10) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ in any given cycle.
- 11) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
- 12) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 13) The Auto-Refresh command interval has been reduced to 3.9 μ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 14) $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 15) $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 16) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.



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- 17) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 18) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.
- 19) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 20) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 = "1") a slow power-down exit timing t_{XARDS} has to be satisfied.

5.7.3 ODT AC Electrical Characteristics

TABLE 31

ODT AC Electrical Characteristics and Operating Conditions for all bins

Symbol	Parameter / Condition			Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 0.7 \text{ ns}$	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measure from t_{AOND} .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} .



6 Specifications and Conditions

TABLE 32
 I_{DD} Measurement Conditions

Parameter	Symbol	Note
Operating Current - One bank Active - Precharge $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, \overline{CSE} is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD0}	1)2)3)4) 5)6)
Operating Current - One bank Active - Read - Precharge $I_{OUT} = 0$ mA, $BL = 4$, $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$, $AL = 0$, $CL = CL(IDD)$; \overline{CSE} is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD1}	1)2)3)4) 5)6)
Precharge Power-Down Current All banks idle; \overline{CSE} is LOW; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable; Data bus inputs are floating.	I_{DD2P}	1)2)3)4) 5)6)
Precharge Standby Current All banks idle; \overline{CSE} is HIGH; \overline{CS} is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are switching, Data bus inputs are switching.	I_{DD2N}	1)2)3)4) 5)6)
Precharge Quiet Standby Current All banks idle; \overline{CSE} is HIGH; \overline{CS} is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable, Data bus inputs are floating.	I_{DD2Q}	1)2)3)4) 5)6)
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, \overline{CSE} is LOW; Other control and address inputs are stable; Data bus inputs are floating. MRS A12 bit is set to "0" (Fast Power-down Exit).	$I_{DD3P(0)}$	1)2)3)4) 5)6)
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, \overline{CSE} is LOW; Other control and address inputs are stable, Data bus inputs are floating. MRS A12 bit is set to 1 (Slow Power-down Exit);	$I_{DD3P(1)}$	1)2)3)4) 5)6)
Active Standby Current All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; \overline{CSE} is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD3N}	1)2)3)4) 5)6)
Operating Current Burst Read: All banks open; Continuous burst reads; $BL = 4$; $AL = 0$, $CL = CL(IDD)$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; \overline{CSE} is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching; $I_{OUT} = 0$ mA.	I_{DD4R}	1)2)3)4) 5)6)
Operating Current Burst Write: All banks open; Continuous burst writes; $BL = 4$; $AL = 0$, $CL = CL(IDD)$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; \overline{CSE} is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD4W}	1)2)3)4) 5)6)
Burst Refresh Current $t_{CK} = t_{CK(IDD)}$; Refresh command every $t_{RFC} = t_{RFC(IDD)}$ interval, \overline{CSE} is HIGH, \overline{CS} is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5B}	1)2)3)4) 5)6)
Distributed Refresh Current $t_{CK} = t_{CK(IDD)}$; Refresh command every $t_{REFI} = 7.8$ μ s interval, \overline{CSE} is LOW and \overline{CS} is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5D}	1)2)3)4) 5)6)



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Parameter	Symbol	Note
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{\text{CK}}$ at 0 V; Other control and address inputs are floating, Data bus inputs are floating.	I_{DD6}	1)2)3)4) 5)6)
Operating Bank Interleave Read Current 1. All banks interleaving reads, $I_{\text{OUT}} = 0 \text{ mA}$; BL = 4, CL = $\text{CL}_{(\text{IDD})}$, AL = $t_{\text{RCD}(\text{IDD})} - 1 \times t_{\text{CK}(\text{IDD})}$; $t_{\text{CK}} = t_{\text{CK}(\text{IDD})}$, $t_{\text{RC}} = t_{\text{RC}(\text{IDD})}$, $t_{\text{RRD}} = t_{\text{RRD}(\text{IDD})}$; CKE is HIGH, $\overline{\text{CS}}$ is HIGH between valid commands. Address bus inputs are stable during deselects; Data bus is switching.	I_{DD7}	1)2)3)4) 5)6)7)

- 1) $V_{\text{DDQ}} = 2.0 \text{ V} \pm 0.1 \text{ V}$; $V_{\text{DD}} = 2.0 \text{ V} \pm 0.1 \text{ V}$
- 2) I_{DD} specifications are tested after the device is properly initialized.
- 3) I_{DD} parameter are specified with ODT disabled.
- 4) Data Bus consists of DQ, DM, DQS, $\overline{\text{DQS}}$, LDQS, $\overline{\text{LDQS}}$, UDQS and $\overline{\text{UDQS}}$.
- 5) Definitions for I_{DD} : see **Table 33**
- 6) Timing parameter minimum and maximum values for I_{DD} current measurements are defined in chapter 7..
- 7) A = Activate, RA = Read with Auto-Precharge, D=DESELECT

TABLE 33
Definition for I_{DD}

Parameter	Description
LOW	defined as $V_{\text{IN}} \leq V_{\text{IL}(\text{ac})\text{MAX}}$
HIGH	defined as $V_{\text{IN}} \geq V_{\text{IH}(\text{ac})\text{MIN}}$
STABLE	defined as inputs are stable at a HIGH or LOW level
FLOATING	defined as inputs are $V_{\text{REF}} = V_{\text{DDQ}} / 2$
SWITCHING	defined as: Inputs are changing between high and low every other clock (once per two clocks) for address and control signals, and inputs changing between high and low every other clock (once per clock) for DQ signals not including mask or stobes



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TABLE 34
 I_{DD} Specification

Speed Grade	-20	-22	-25	-28	-33	Unit	Note
Symbol	typ.	typ.	typ.	typ.	typ.		
I_{DD0}	92	87	81	77	70	mA	
I_{DD1}	99	94	89	85	78	mA	
I_{DD2P}	4	4	4	4	4	mA	
I_{DD2N}	46	43	41	38	33	mA	
I_{DD2Q}	40	38	38	35	31	mA	
$I_{DD3P(0)}$	30	29	28	27	23	mA	1)
$I_{DD3P(1)}$	5	5	5	5	4	mA	2)
I_{DD3N}	52	48	47	43	37	mA	
I_{DD4R}	166	158	153	145	127	mA	
I_{DD4W}	189	173	163	149	129	mA	
I_{DD5B}	127	122	119	115	109	mA	
I_{DD5D}	5	5	5	5	4	mA	3)
I_{DD6}	4	4	4	4	3	mA	3)
I_{DD7}	204	204	193	193	179	mA	

1) MRS(12)=0

2) MRS(12)=1

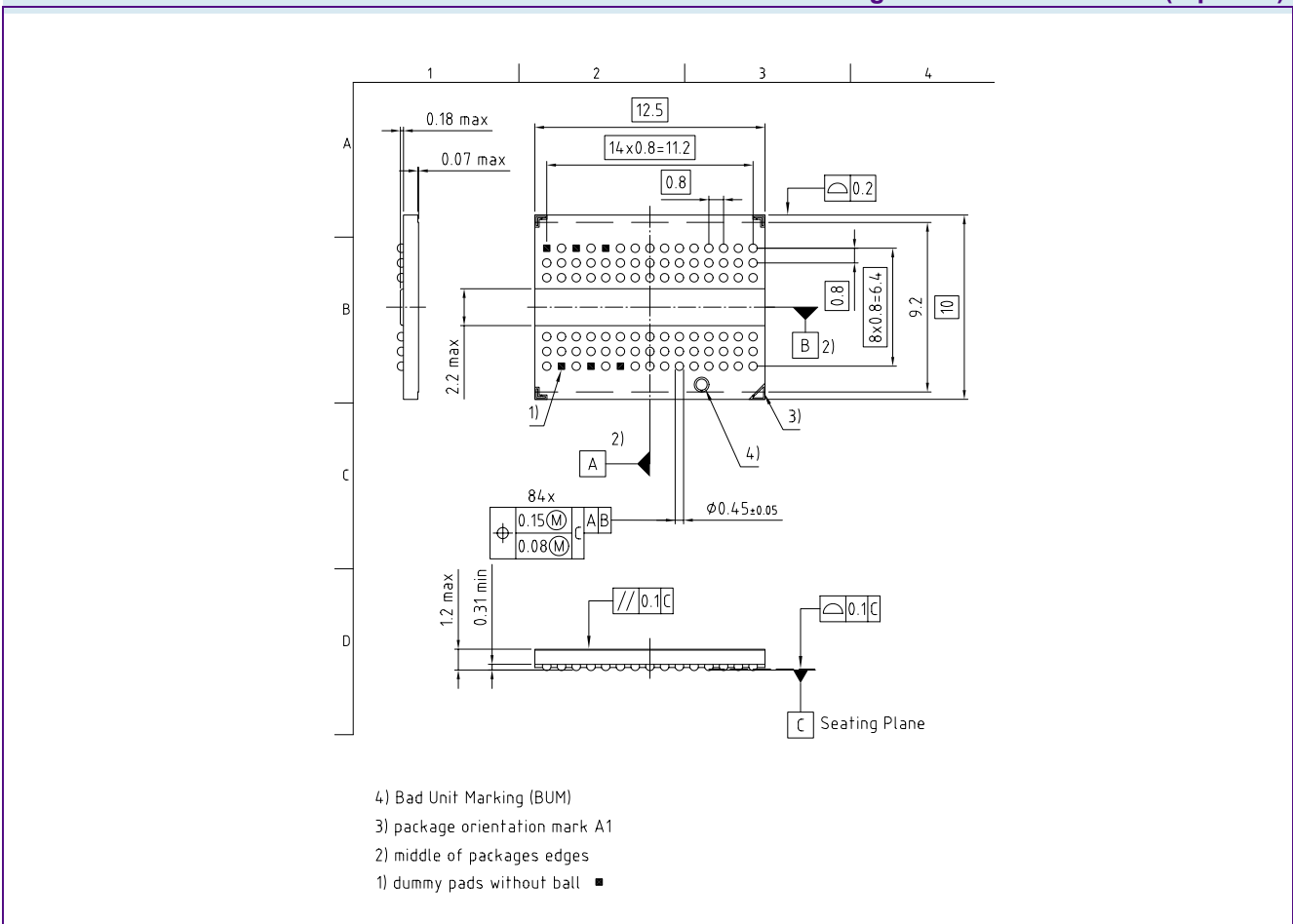
3) $0 \leq T_{CASE} \leq 85^{\circ}C$



7 Package

7.1 Package Dimension

FIGURE 6
Package Outline P-TFBGA-84 (top view)





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7.2 Package Thermal Characteristics

TABLE 35
Package thermal characteristics

JESD51	Theta _{jA} ¹⁾						Theta _{jC} ²⁾
Industrial standard Board	1s0p			2s0p			
Air Flow	0 m/s	1 m/s	3 m/s	0 m/s	1 m/s	3 m/s	—
Rth[K/W]	69	53	47	41	35	33	5

- 1) Junction to Ambient thermal resistance. The value has been obtained by simulation using the conditions stated in the Industrial standard JESD-51 standard.
- 2) Junction to Case thermal resistance. The value has been obtained by simulation.



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